ABSTRACT OF THE DISCLOSURE

A method implements a change to a circuit design for a system formed on a semiconductor chip, the circuit design including at least one circuit core. The method includes providing in the circuit design at least one field programmable gate array (FPGA) core, extracting an incremental change to the circuit design by comparing a new resister-transfer-level (RTL) design and an old RTL design for the system, synthesizing the incremental change into a netlist for the at least one FPGA core, generating new metal layer interconnections so as to provide an input and an output for the at least one FPGA core in accordance with the incremental change, and programming the at least one FPGA core in accordance with the netlist. The at least one FPGA core is provided in an otherwise unused area of the chip.